

REMARKS

The present application was filed on September 30, 2003 with claims 1-20. Claims 1-20 were pending in the application prior to the amendments herein. Claims 1, 19 and 20 are the pending independent claims.

Claims 1-20 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,764,641 (hereinafter "Lin").

In this response, Applicant amends independent claims 1, 19 and 20, and cancels dependent claim 6. Applicant respectfully requests reconsideration of the present application in view of the amendments above and remarks below.

Independent claim 1 has been amended to indicate that the controller circuitry is operative to maintain separate discarded data block indicators for respective ones of the plurality of input ports. This limitation is similar to that in originally-filed dependent claim 6, which is now canceled.

In an illustrative embodiment of the invention, described in the specification at page 10, lines 5-11, the controller 204 in network processor 102 as shown in FIG. 2 maintains separate state bits for each of the N input ports 200-1 through 200-N in the set of input ports 200. See steps 304 through 308 of the flow diagram in FIG. 3. As indicated at page 7, lines 11-13, such an approach advantageously reduces the number of PDUs that are corrupted via discarded data blocks in an oversubscription condition, thereby improving processor throughput and performance. It is to be appreciated, of course, that these particular aspects of the illustrative embodiment are presented by way of example only, and are not to be construed as limitations of the claimed invention.

In characterizing the Lin reference as allegedly meeting certain limitations of dependent claim 6 as originally filed, the Examiner relies primarily on column 6, lines 55-61, and FIG. 3B, steps 111-112, of Lin. However, Applicant respectfully submits that the relied-upon portions of Lin fail to anticipate the limitations as alleged. The Lin reference, in column 6, lines 55-61, states the following, with emphasis supplied:

If the queue length exceeds the EPD buffer threshold, the controller 18 discards the cell, since the controller cannot ensure that it will have available sufficient buffer space to hold the remaining cells of the packet as they arrive. The controller thus pre-

empties what is expected to be a fragmented packet. The controller then sets an EPD flag that is associated with the virtual circuit identified in the cell (steps 111-112).

The Examiner apparently argues that the early packet discard (EPD) flag of Lin is anticipatory of the recited discarded data block indicator. However, claim 1 as amended indicates that separate such indicators are maintained for respective input ports of the processor. The relied-upon portions of Lin indicate that EPD flags are set for particular virtual circuits that are identified in a corresponding cell. This not only fails to teach or suggest the claimed arrangement, but appears to actively teach away from it. Moreover, it fails to provide the above-noted advantages in terms of providing a particularly efficient mechanism for reducing the number of PDUs that are corrupted via discarded data blocks in an oversubscription condition.

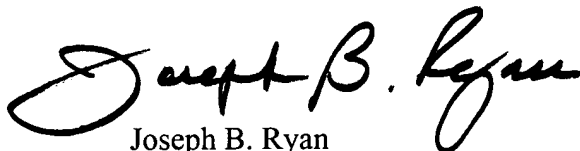
Accordingly, it is believed that the teachings of Lin fail to meet the limitations of amended claim 1.

Independent claims 19 and 20 as amended include limitations similar to those of claim 1, and are therefore believed allowable for reasons similar to those described above with reference to claim 1.

Dependent claims 2-5 and 7-18 are believed allowable for at least the reasons identified above with regard to claim 1.

In view of the foregoing, claims 1-5 and 7-20 are believed to be in condition for allowance.

Respectfully submitted,



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Joseph B. Ryan
Attorney for Applicant(s)
Reg. No. 37,922
Ryan, Mason & Lewis, LLP
90 Forest Avenue
Locust Valley, NY 11560
(516) 759-7517